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The Engineer's Guide To EMI In DC-DC Converters (Part 3): Understanding Power Stage Parasitics

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The high-frequency switching of semiconductor devices in dc-dc converters represents a significant source of conducted and radiated emissions. Part 2 of this article series[1, 2] provided a review of differential-mode (DM) and common-mode (CM) conducted noise disturbances from dc-dc converters. By separating the DM and CM noise components from the total noise measurement during electromagnetic interference (EMI) testing, you can distinguish between DM and CM contributions and thus simplify the EMI filter design process. CM noise in particular can dominate conducted emissions at high frequencies and, given the large conducting loop areas, represents a greater contribution to the generation of radiated emissions.

In part 3, I'll provide a comprehensive illustration of inductive and capacitive parasitic elements for a buck regulator circuit that affect not only EMI performance but also switching losses. By understanding the contribution of the responsible circuit parasitics, you can take steps to minimize them and reduce the overall EMI signature. In general, a compact, optimized power-stage layout not only lowers EMI for easier regulatory compliance, but also increases efficiency and reduces overall solution cost.

Examining Critical Loops With High-Slew-Rate Currents

In translating a power-supply schematic to a board layout, one essential step is to pinpoint the high slew-rate current (high di/dt) loops, with an eye to identifying the layout-induced parasitic or stray inductances that cause excessive noise, ringing, overshoot and ground bounce. The power-stage schematic in Fig. 1 shows a synchronous buck controller driving high-side and low-side MOSFETs designated as Q_1 and Q_2, respectively.

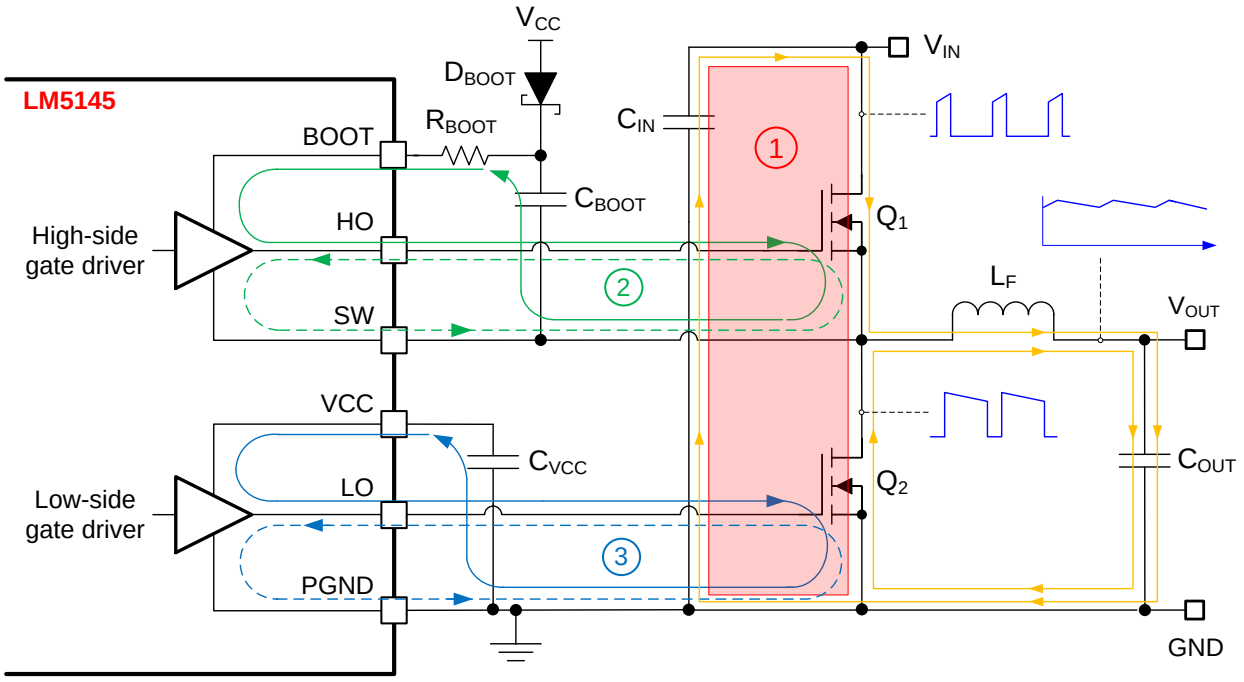


Fig. 1. Critical high-frequency switching loops with high slew-rate currents in a buck converter power stage.

Consider the turn-on transition of Q_1. Supplied by the input capacitor C_{IN}, Q_1's drain current increases rapidly to the inductor current level while the current flowing from Q_2's source to drain drops to zero. In Fig. 1, the loop shaded in red, which is formed by the MOSFETs and input capacitor and labeled "1", is the buck regulator's high-frequency commutating power loop, or "hot" loop.[3,4] The power loop carries high-frequency currents of relatively large amplitude and di/dt, particularly during MOSFET switching.

Loops 2 and 3 in Fig. 1 are classified as gate loops for the power MOSFETs. More specifically, loop 2 represents the high-side MOSFET's gate-driver circuit supplied by the bootstrap capacitor, C_{BOOT}. Likewise, loop 3 corresponds to the low-side MOSFET's gate driver supplied by V_{CC}. The turn-on and turn-off gate-current paths are delineated in each case by solid and dashed lines, respectively.

Parasitic Components And Radiated EMI

EMI problems typically entail three elements—source, victim and coupling mechanism. The source refers to a noise generator with high dv/dt and/or di/dt, and the victim corresponds to a susceptible circuit (or the EMI measurement equipment).

Coupling mechanisms can be categorized into conductive and nonconductive coupling. Non-conductive coupling can be electric field (E-field) coupling, magnetic field (H-field) coupling or a combination of both. This occurs as a result of parasitic inductances and capacitances and may have a decisive and significant effect on a regulator's EMI performance.

Power-Stage Parasitic Inductances

Power MOSFET switching behavior and the consequences for waveform ringing and EMI correlate with the partial inductances[5] of the power loop and gate-drive circuits. Fig. 2 provides a comprehensive illustration of the parasitic elements arising from component placement, device package and printed circuit board (PCB) layout routing that affect synchronous buck regulator EMI performance.

The effective high-frequency power-loop inductance, L_{LOOP}, is a sum of the total drain inductance, L_D, and common-source inductance, L_S, resulting from the equivalent series inductance (ESL) of the input capacitor and PCB traces and the package inductances of the power MOSFETs. As expected, L_{LOOP} is highly related to the layout geometry of the input capacitor-MOSFET loop, denoted by the red-shaded area in Fig. 1.[6, 7, 8]

Meanwhile, the self-inductance, L_G, of the gate loop includes lumped contributions from the MOSFET package and PCB trace routing. An inspection of Fig. 2 reveals that the common-source inductance of the high-side MOSFET Q_1 exists mutually in both the power and gate loops. Common-source inductance of Q_1 reduces the di/dt in the power loop because it creates an opposing feedback voltage effect that impedes the rise and fall times of the MOSFET's gate-source voltage. However, it has the detrimental effect of increasing switching loss and is thus undesirable.[9, 10]

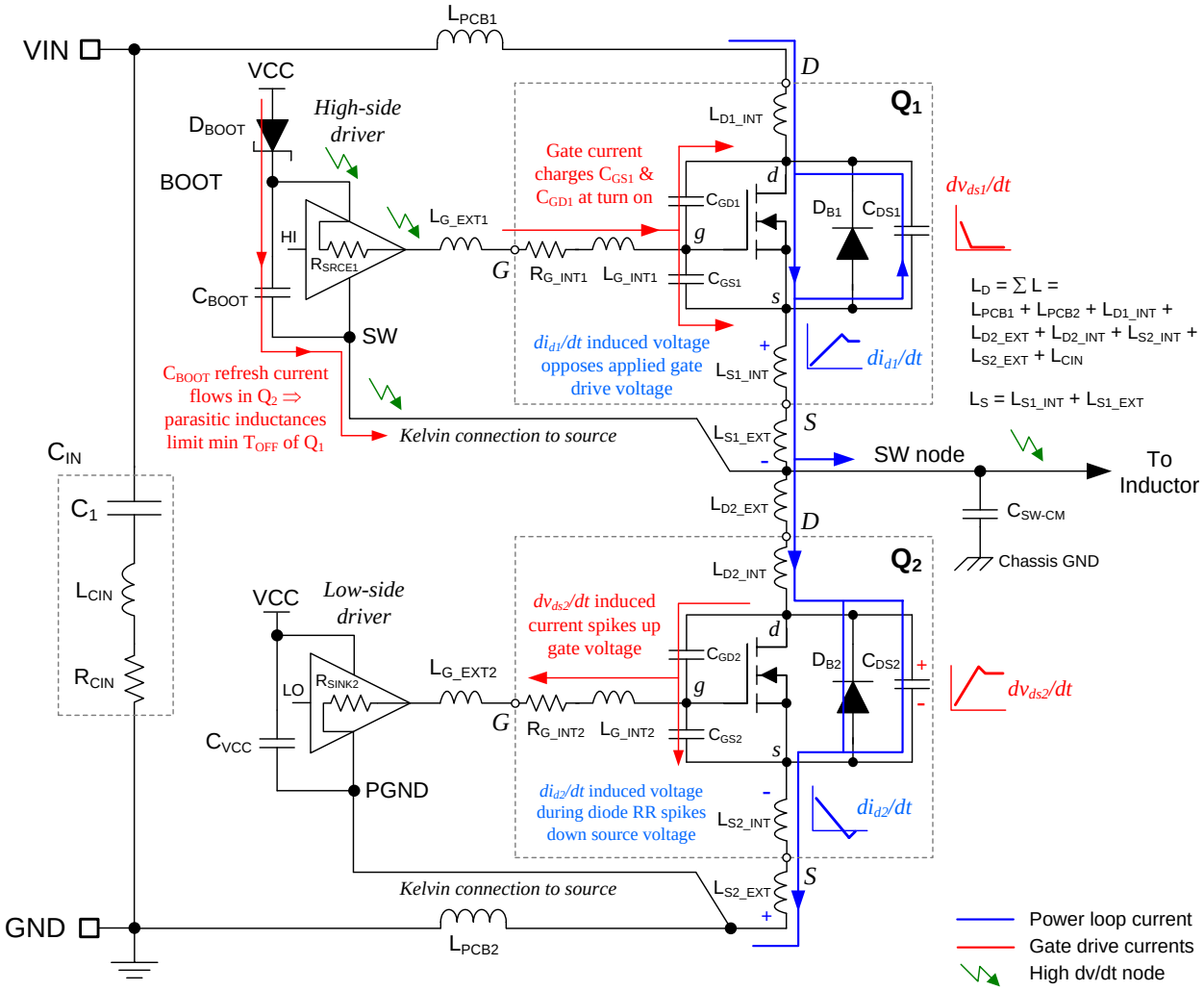


Fig. 2. Buck power stage and gate driver "hidden schematic" inclusive of inductive and capacitive parasitic elements.

Power-Stage Parasitic Capacitances

Equation 1 expresses the power MOSFET input, output and reverse-transfer capacitances that affect EMI and switching behaviors as a function of the terminal capacitances shown in Fig. 2. Such internal MOSFET capacitances demand high-amplitude, high-frequency currents during switching transitions.

$$C_{ISS} = C_{GS} + C_{GD}$$
$$C_{OSS} = C_{DS} + C_{GD} \qquad (1)$$
$$C_{RSS} = C_{GD}$$

Equation 2's approximation shows a highly nonlinear voltage dependency for C_{OSS}. Equation 3 gives the effective charge Q_{OSS} at a particular input voltage, where $C_{OSS\text{-}TR}$ is the time-related effective output capacitance as defined in the data sheets of some newer power FET devices.[11]

$$C_{OSS}(v_{DS}) \approx C_{OSS,ref}\sqrt{\frac{v_{DS,ref}}{v_{DS}}} \quad (2)$$

$$Q_{OSS}(V_{IN}) = \int_0^{V_{IN}} C_{OSS}(v)dv = V_{IN} \cdot C_{OSS\text{-}TR}(V_{IN}) \quad (3)$$

Another critical parameter from Fig. 2 is the reverse-recovery charge of body diode D_{B2}, designated as Q_{RR}, causing a significant spike in the current of Q_1 during turn-on. Q_{RR} depends on many parameters, including diode forward current prior to recovery, current transition speed and die temperature. In general, MOSFET Q_{OSS} and body diode Q_{RR} present several challenges to both analysis and measurement. The leading-edge current spikes during turn-on of Q_1 to charge C_{OSS2} of Q_2 and supply Q_{RR2} to recover body diode D_{B2} have similar profiles, and the two are often conflated.

EMI Frequency Ranges And Coupling Modes

Delineated in Table 1 are the three loosely defined frequency ranges over which a switch-mode power converter excites and propagates EMI.[6] During power MOSFET switching, when the slew rate of the commutating current can exceed 5 A/ns, a 2-nH parasitic inductance results in a voltage overshoot of 10 V. Furthermore, the current in the power loop with fast switching edges—and possible leading-edge ringing related to body diode reverse recovery and MOSFET C_{OSS} charging—is rich in harmonic content, posing a severe threat of H-field coupling and consequently increased conducted and radiated EMI.

Table 1. Switching converter noise sources and general EMI frequency classifications.

Converter noise type		Dominant converter noise source	EMI frequency range	Conducted/radiated emissions
1	Low-frequency noise	Switching frequency harmonics	150 kHz to 50 MHz	Conducted
2	Broadband noise	MOSFET voltage and current rise/fall times, resonant ringing	50 MHz to 200 MHz	Both
3	High-frequency noise	Body diode reverse recovery	Above 200 MHz	Radiated

The three dominant noise-coupling paths are conducted noise through the dc input lines, H-field coupling from the power loop and inductor, and E-field coupling from the switch-node copper surface.[8]

Analytical Modeling Of Converter Switching Waveform

As highlighted in part 2, the switch-node voltage rising and falling edges represent the dominant source of CM noise and E-field coupling in nonisolated converters. In EMI analysis, the upper bound or "spectral envelope" of the harmonic content of the noise emissions of a power converter, as opposed to the amplitudes of individual harmonic components, is of most interest to designers. Simplified analytical models of switching waveforms allow you to readily establish the influence of time-domain waveform parameters on the resulting frequency spectrum.

To get an idea of the harmonic frequency spectral envelope pertaining to the switch-node voltage, Fig. 3 approximates the time-domain waveform. Each segment is characterized by its amplitude (V_{IN}), duty cycle (D), rise and fall times (t_R and t_F), and pulse width (t_1), defined between the midpoints of the rising and falling edges.

Fourier analysis reveals that the harmonic amplitude envelope is a double-sinc function with corner frequencies of f_1 and f_2, depending on the pulse width and rise/fall time of the time-domain waveform.[12] You can apply a similar treatment for the trapezoidal MOSFET current waveforms of the buck switching cell. The applicable frequency component(s) from the measured voltage and current waveforms can represent a ringing characteristic at the edges of the switch voltage and current waveforms (arising from parasitic loop inductance and body diode reverse recovery, respectively).

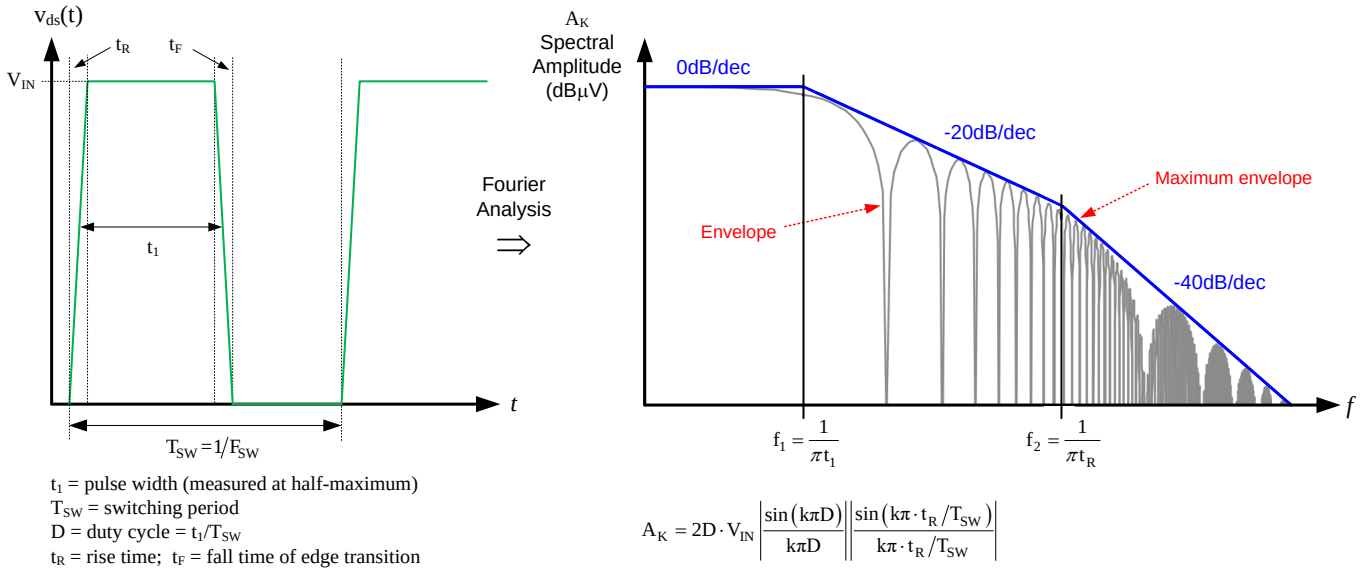


Fig. 3. Switch-node voltage trapezoidal waveform and its spectral envelope impacted by pulse width and rise/fall times.

In general, inductance L_{LOOP} increases the MOSFET drain-to-source peak voltage spike. It also exacerbates switch-node voltage ringing, affecting broadband EMI in the 50-MHz to 200-MHz range. Clearly, then, it is vital to minimize the effective loop length and enclosed area of the power loop. Not only does this reduce parasitic inductance, but magnetic field self-cancellation is possible using an image ground plane to reduce the magnetically coupled radiated energy emanating from what effectively is a loop antenna structure.

Conducted noise occurs on the input side of the buck regulator based on the ratio of loop inductance and input capacitor ESL. Fortunately, the noise conducted to the output is minimal if the buck output inductor has a high self-resonant frequency (SRF). In other words, the inductor should have a low effective parallel capacitance (EPC) to obtain a high transfer impedance from switch node to V_{OUT} nets. The output noise is additionally filtered by low-impedance output capacitor(s).

Equivalent Resonant Circuits

Looking at the synchronous buck regulator time-domain switch-node voltage waveform in Fig. 4, the parasitic energy transferred during MOSFET switching excites RLC resonance. Simplified equivalent circuits are captioned for analyzing the switching behavior when Q_1 turns on and off. Switch-node voltage overshoot above V_{IN} and undershoot below ground (GND) are evident during the rising and falling edges of the voltage waveform, respectively.

The oscillation amplitude depends on the distribution of partial inductances within the loop, and the effective ac resistance of the loop damps the subsequent ringing. Not only does this contribute to voltage stress on the MOSFETs and gate drivers; it also correlates to the frequency at which broadband radiated EMI is centered.

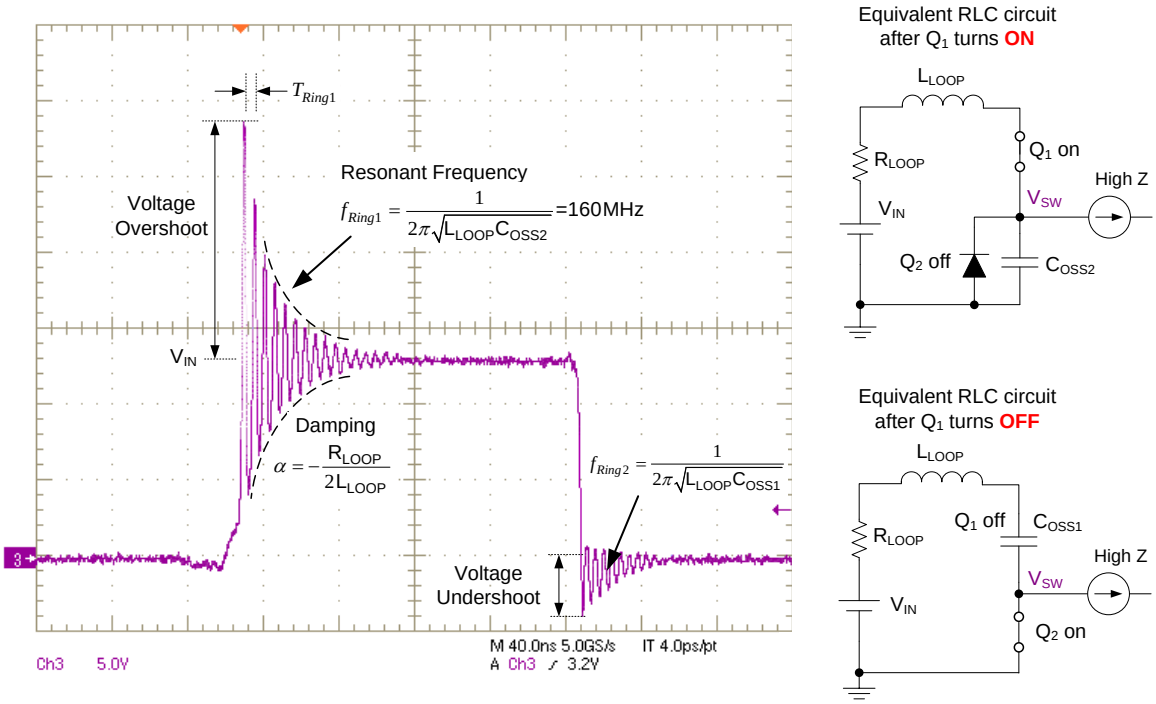


Fig. 4. Synchronous buck switch-node voltage waveform and equivalent RLC circuits during MOSFET turn-on and turn-off switching transitions.

Rising edge voltage overshoot indicates a ringing period of 6.25 ns in Fig. 4, corresponding to a resonant frequency of 160 MHz. A near-field H-probe placed directly over the switching loop area also identifies this frequency component. Computational EM field simulation tools[13] can derive the partial loop inductance values associated with the high-frequency resonance and radiated emission. However, a simpler technique involves measuring resonant period T_{Ring1}, and knowing C_{OSS2} at the input voltage operating point from the MOSFET's data sheet, equation 4 calculates the total loop inductance.

$$\sum L_{LOOP} = \frac{T_{Ring1}^{2}}{4\pi^{2}C_{OSS2}} \qquad (4)$$

Two important aspects are the resonant frequency and the loss or damping factor α inherent to the resonance. The main design goal is to push the resonant frequency as high as possible by minimizing the loop inductance. This decreases the total stored reactive energy and lowers the resonant switch-node voltage peak overshoot. Also, the damping factor increases at higher frequencies due to the skin effect, increasing the effective value of R_{LOOP}.

Summary

Gallium nitride (GaN) power stages[7,10,11] notwithstanding, low to medium voltage synchronous buck and boost converters generally switch at frequencies under 3 MHz but generate broadband noise and EMI to 1 GHz and above. The major source of EMI is due to the nature of their fast-switching voltages and currents. In fact, the high-frequency spectral content of the device switching waveforms is an alternative means of obtaining an indication of the EMI generation potential and points to a tradeoff of EMI against switching loss.

Starting with an awareness of the key converter switching loops from the schematic and diligently minimizing the areas of these loops during PCB layout design will inevitably abate parasitic inductance and related H-field coupling, leading to lower conducted and radiated EMI.

In a subsequent installment of this article series, I'll present results for several dc-dc converter circuits that highlight both system-level and integrated circuit (IC)-specific features to improve the EMI performance vector. Measures to mitigate conducted EMI can also improve radiated EMI: the two aspects are frequently reciprocal.

References

1. "The Engineer's Guide To EMI In DC-DC Converters (Part 1): Standards Requirements And Measurement Techniques" by Timothy Hegarty, How2Power Today, December 2017 issue.

2. "The Engineer's Guide To EMI In DC-DC Converters (Part 2): Noise Propagation And Filtering" by Timothy Hegarty, How2Power Today, January 2018 issue.

3. Achieving low noise and low EMI performance with DC/DC switching regulators, Texas Instruments EMI landing page.

4. LM5145 6-V to 75-V Synchronous Buck DC/DC Controller with Wide Duty Cycle Range (cf. power stage layout guidelines), Texas Instruments Data Sheet SNVSA14, June 2017.

5. "Inductance: Loop and Partial" by Clayton R. Paul, (Hoboken, New Jersey: Wiley-IEEE Press, 2009).

6. "DC/DC buck converter EMI reduction using PCB layout modification" by Ankit Bhargava, David Pommerenke, Keong W. Kam, Federico Centola, and Cheng Wei Lam. IEEE Transactions on Electromagnetic Compatibility (August 2011), pp. 806-813.

7. "Layout considerations for LMG5200 GaN Power Stage" by Narendra Mehta, Texas Instruments Application Note SNVA729 (September 2015).

8. "EMC guideline for synchronous buck converter design" by Keong Kam, David Pommerenke, Federico Centola, Cheung-Wei Lam, and Robert Steinfeld, IEEE International Symposium on Electromagnetic Compatibility (August 2009), pp. 47-52.

9. "Controlling switch-node ringing in synchronous buck converters" by Robert Taylor and Ryan Manack, Texas Instruments Analog Applications Journal SLYT465 (2Q 2012): pp. 5-7.

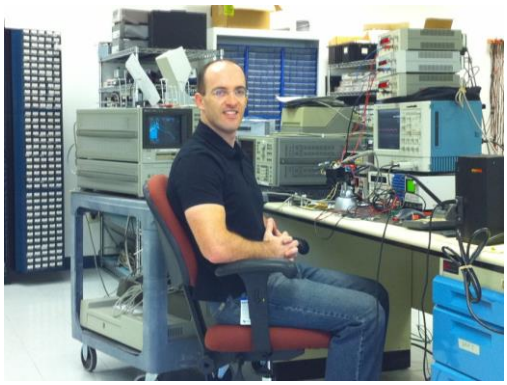
10. "A multiloop method for minimization of parasitic inductance in GaN-based high-frequency DC/DC converter" by Kangping Wang, Laili Wang, Xu Yang, Xiangjun Zeng, Wenjie Chen, and Hongchang Li, IEEE Transactions on Power Electronics (June 2017), pp. 4728-4740.

11. "Comparison of deadtime effects on the performance of DC/DC converters with GaN FETs and silicon MOSFETs" by John S. Glaser and David Reusch, 2016 IEEE Energy Conversion Congress and Exposition (September 2016), pp. 1-8.

12. "Analysis of shaped pulse transitions in power electronics switching waveforms for reduced EMI generation" by Niall Oswald, Bernard Stark, Derrick Holliday, Collin Hargis, and Bill Drury, IEEE Transactions on Industry Applications (Sept. 2011), pp. 2154-2165.

13. "Investigation of EM field coupling from DC/DC buck converters to automobile AM-FM antennas" by Cyrous Rostamzadeh, Patrick DeRoy, Andreas Barchanski, and Behrouz Abdolali, 2016 IEEE International Symposium on Electromagnetic Compatibility (July 2016), pp. 364-369.

About The Author



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Tim's current focus is on enabling technologies for high-frequency, low-EMI, isolated and nonisolated regulators with wide input voltage range, targeting industrial, communications and automotive applications in particular. He is a senior member of the IEEE and a member of the IEEE Power Electronics, Industrial Applications and EMC Societies.

For more information on EMI, see How2Power's Power Supply EMI Anthology. Also see the How2Power's Design Guide, locate the Design Area category and select "EMI and EMC".